REMARKS

Claims 1-16 are currently pending. Claims 1-11 are currently being considered, of which claims 1 and 11 have been amended. Claims 12-16 stand withdrawn. No new claims have been added, and no new matter has been introduced.

Claims 8 and 10 are objected to as being dependent upon a rejected base claim. The Examiner has indicated that claims 8 and 10 would be allowed if rewritten in independent form including all the limitations of the base claim and any intervening claims. Applicant appreciates this indication of allowable subject matter in claims 8 and 10, and respectfully requests that the Examiner hold this objection in abeyance while considering the remarks herein.

The Examiner has suggested that the title of the invention is not descriptive, and has required a new title that is clearly indicative of the invention to which the claims are directed. Applicant has amended the title to be "QUANTUM SEMICONDUCTOR DEVICE HAVING A QUANTUM DOT AND METHOD FOR FABRICATING THE QUANTUM SEMICONDUCTOR DEVICE". Thus, Applicant respectfully submits that the Examiner's requirement for a new title should be withdrawn.

Claims 1-7, 9, and 11 stand rejected under 35 USC 102(b) as anticipated by USP 5,559,343 **(Kiehl)**.

Applicant respectfully traverses this rejection.

Kiehl discloses a semiconductor device comprising: a n-type GaAs layer (source layer) 12 formed on a semi-insulating GaAs substrate 11; a multi-layer structure of p-type AlGaAs layers 13a-13d and GaAs layers 14a-14c formed on the n-type GaAs layer 12; arsenic precipitates 21a-21c formed in the GaAs layers 14a-14c respectively; a n-type InGaAs layer 16 formed on the multi-layer structure; a WSi electrode (WSi stressor) 17 formed on the n-type InGaAS layer 16; a dielectric layer 23 of SiO_2 formed on side surfaces of a mesa structure; a drain electrode 25a formed on the WSi electrode 17; gate electrodes 25b, 25c formed on both sides of the mesa structure with the dielectric layer 23 therebetween; and a source electrode 26 connected to the n-type GaAs layer (source layer) 12 (FIGs. 8A-8G).

The precipitates 21 form Schottky contact with the GaAs layers 14 and also with the AlGaAs layers 13. Since the barrier layer 13 between adjacent pair of precipitates 21 are sufficiently narrow, a charge on one precipitate 21 can tunnel through the barrier layer 13 to the adjacent precipitate 21. Such tunneling can be controlled by potential distribution in the superlattice structure 13, 14. The potential of the precipitates 21 can be controlled by the voltage applied to the gate electrode 25b, 25c. In **Kiehl**, the tunnel current flows in a direction perpendicular to the surface of the substrate 11.

The present invention is clearly different from **Kiehl**.

(1) A first issue is as follows. According to the principles disclosed in the present application, a two-dimensional carrier gas 19 is formed in a first semiconductor layer 18 (see FIGs. 5A and 5B of the present application). The reason that the two-dimensional carrier gas 19 is formed in the first semiconductor layer 18 is for forming a channel region 29 in the first semiconductor layer 18 (see FIGs. 1-2B of the present application).

The Examiner has suggested that the GaAs 14a of **Kiehl** corresponds to a first semiconductor layer as claimed in the present application.

However, the GaAs layer 14a of **Kiehl** does not correspond to a first semiconductor layer as claimed in the present application. The GaAs layer 14a is only a matrix of the arsenic precipitates 21a. A two-dimensional carrier gas is not formed in the GaAs layer 14a. Since the tunneling current flows in the direction perpendicular to the surface of the substrate 11, there is no need to form the two-dimensional carrier gas in the GaAs layer 14a.

Thus, Applicant respectfully believes that the Examiner's suggestion is incorrect, regarding this first issue.

(2) A second issue is as follows. According to the principles disclosed in the present application, oxide layers 26a, 26b are formed on both sides of a dot-shaped structure 24 on the upper surface of the second semiconductor layer 22 (see FIGs. 1-2B of the present application). The reason that the oxide layers 26a, 26b are formed on both sides of the dot-shaped structure 24 on the upper surface of the second semiconductor layer 22 is for forming depletion regions 28a, 28b in regions of the first semiconductor layer 18 below the oxide layers 26a, 26b. In the present application, a channel region is defined by the depletion regions 28a, 28b.

The Examiner has suggested that the dielectric layer 23 of **Kiehl** corresponds to oxide layers as claimed in the present application.

However, the dielectric layer 23 of **Kiehl** does not correspond to the oxide layers as claimed in the present application. The dielectric layer 23 of **Kiehl** is for insulating the gate electrodes 25b, 25c from the mesa structure. The dielectric layer 23 of **Kiehl** is not for forming a depletion region in the GaAs layer 14a. Furthermore, the dielectric layer 23 of **Kiehl** is formed on the side surfaces of the GaAs layer 14b (see FIG. 8G).

Thus, Applicant respectfully believes that the Examiner's suggestion is incorrect, regarding this second issue.

(3) A third issue is as follows. According to the principles disclosed in the present application, a dot-shaped structure 24 is formed on the surface of the second semiconductor layer 22 at a position above the quantum dot 20, and the oxide layers 26a, 26b are formed on both sides of the dot-shaped structure 24 with the dot-shaped structure 24 as a mark (see FIGs. 1-2B of the present application). Since the dot-shaped structure 24 is formed on the surface of the second semiconductor layer 22 at a position above the quantum dot 20, it is possible to form oxide layers 26a, 26b with the dot-shaped structure 24 as the mask. Therefore, it is possible to form the depletion regions 28a, 28b on both sides of the quantum dot 20, although the quantum dot 20 is buried in the second semiconductor layer 22.

Kiehl fails to describe, teach, or suggest such a technique of the present application.

The Examiner has suggested that the precipitate 21b of **Kiehl** corresponds to a dot-shaped structure as claimed in the present application.

However, the precipitate 21b of **Kiehl** does not correspond to a dot-shaped structure as claimed in the present application. The function of the precipitate 21b is similar to the function of the precipitate 21a. The precipitate 21b does not function as a mark when the dielectric layer 23 is formed.

Thus, Applicant respectfully believes that the Examiner's suggestion is incorrect, regarding this third issue.

Kiehl fails to describe, teach, or suggest the following set forth in claim 1, as amended: "a first semiconductor layer formed over a substrate and having a two-dimensional carrier gas formed in; ... oxide layers formed on both sides of the dot-shaped structure on the upper surface of the second semiconductor layer", in combination with the other claimed features.

Kiehl fails to describe, teach, or suggest the following set forth in claim 11, as amended: "forming over a substrate a first semiconductor layer with a two-dimensional carrier gas formed in; ... forming a dot-shaped structure on the surface of the second semiconductor at a position above the quantum dot due to strains generated in the surface of the second semiconductor layer due to the presence of the quantum dot; and forming oxide layers on the upper surface of the second semiconductor layer on both side of the dot-shaped structure with the dot-shaped structure as a mark", in combination with the other claimed features.

Thus, Applicant respectfully submits that this rejection of claims 1-7, 9, and 11 should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, all claims currently being considered are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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